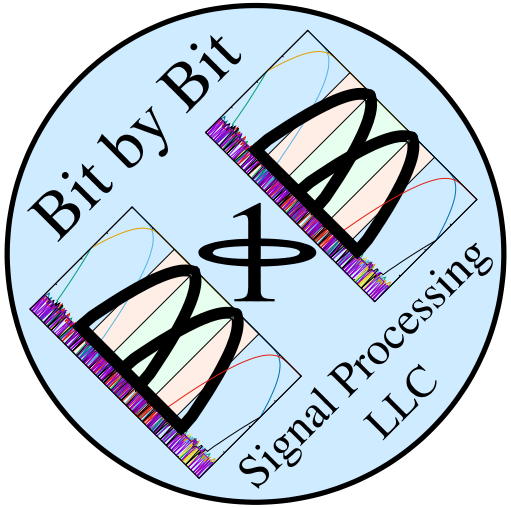


The BxBFFT Advantage

Dr. Ross D. Martin

Bit by Bit Signal Processing LLC

Web: https://bitbybitsp.com
Email: ross@bitbybitsp.com
Phone: +1-623-487-8011

The BxBFFT

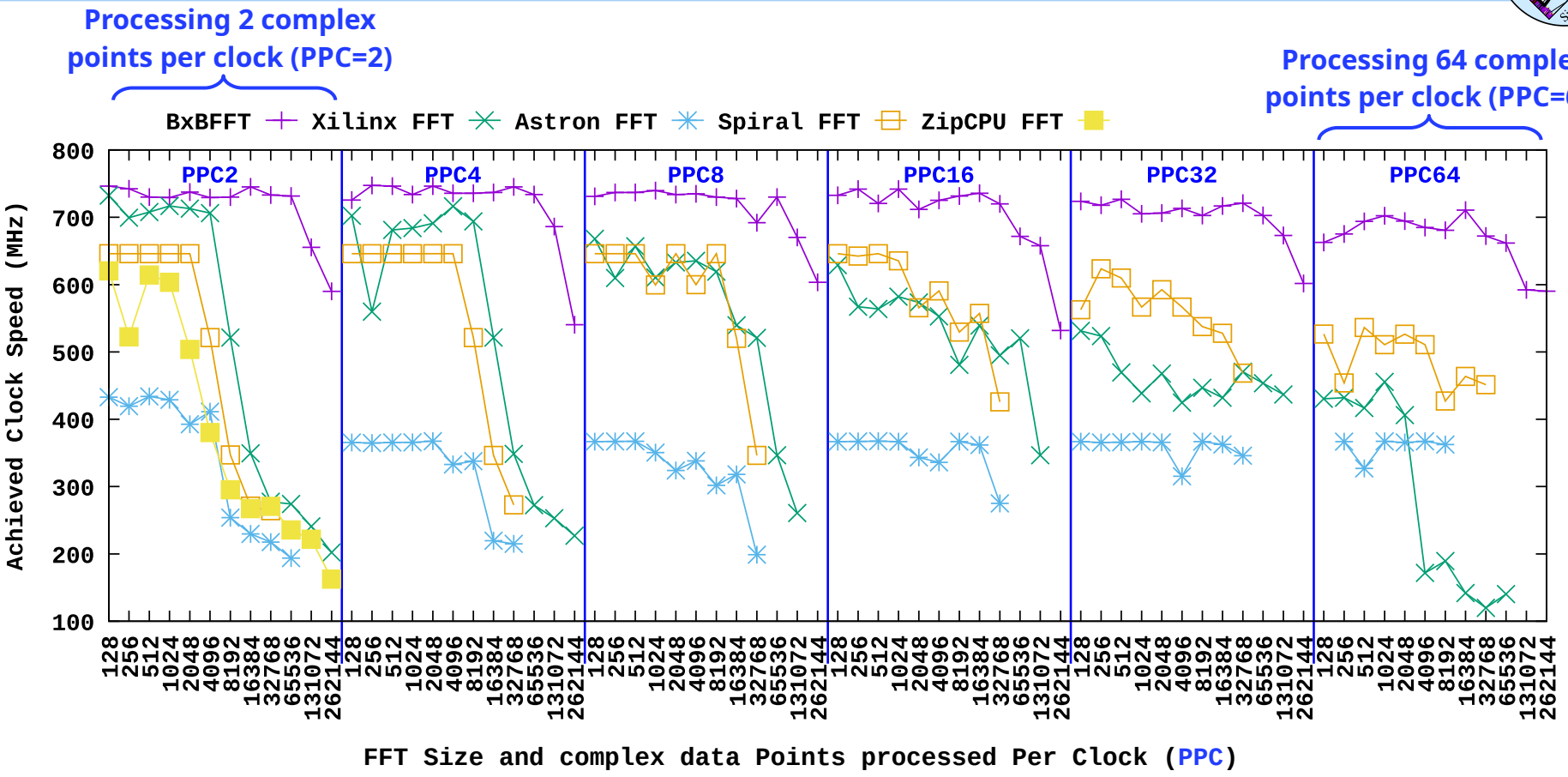
- **A Fast Fourier Transform (FFT)**
- **Optimized for Massive Data Problems**
  - Radar and Lidar
  - Beamformers, Routers, and Repeaters
    - Communication Satellites, Cable TV
  - Spectrum Monitoring and Radio Astronomy
  - MKID photonic sensors
  - Test Equipment and Medical Imaging
  - Cellular front ends, Cellular Backhaul, and FDMA

Problems are tending towards ever larger and faster data. The more data increases, the more you need a BxBFFT to handle that data, because of its **Speed**, **Efficiency**, **Features**, and **Time to Market** advantages.

FFT Comparisons

- **Graphs compare the BxBFFT to other FFTs**
  - The most comprehensive FFT comparison anywhere
  - 18 bit data; Fully Natural data in and out
  - Only basic features enabled; just FFTs with reset
  - Testing is restricted to power-of-2 FFT sizes
- **Not all FFTs support the basic features**
  - Xilinx SSR FFT doesn’t support a reset
  - Altera Parallel FFT only supports bit reversed output
  - The Astron FFT output is only Partially Natural
  - Testing with fewer features gives a false advantage
  - Performance of these FFTs may be artificially good
- **Only the BxBFFT works for all tested sizes**
  - Some FFTs don’t work for high FFT Size
  - Some FFTs don’t work for high Points Per Clock (PPC)
  - In these cases, data points are missing

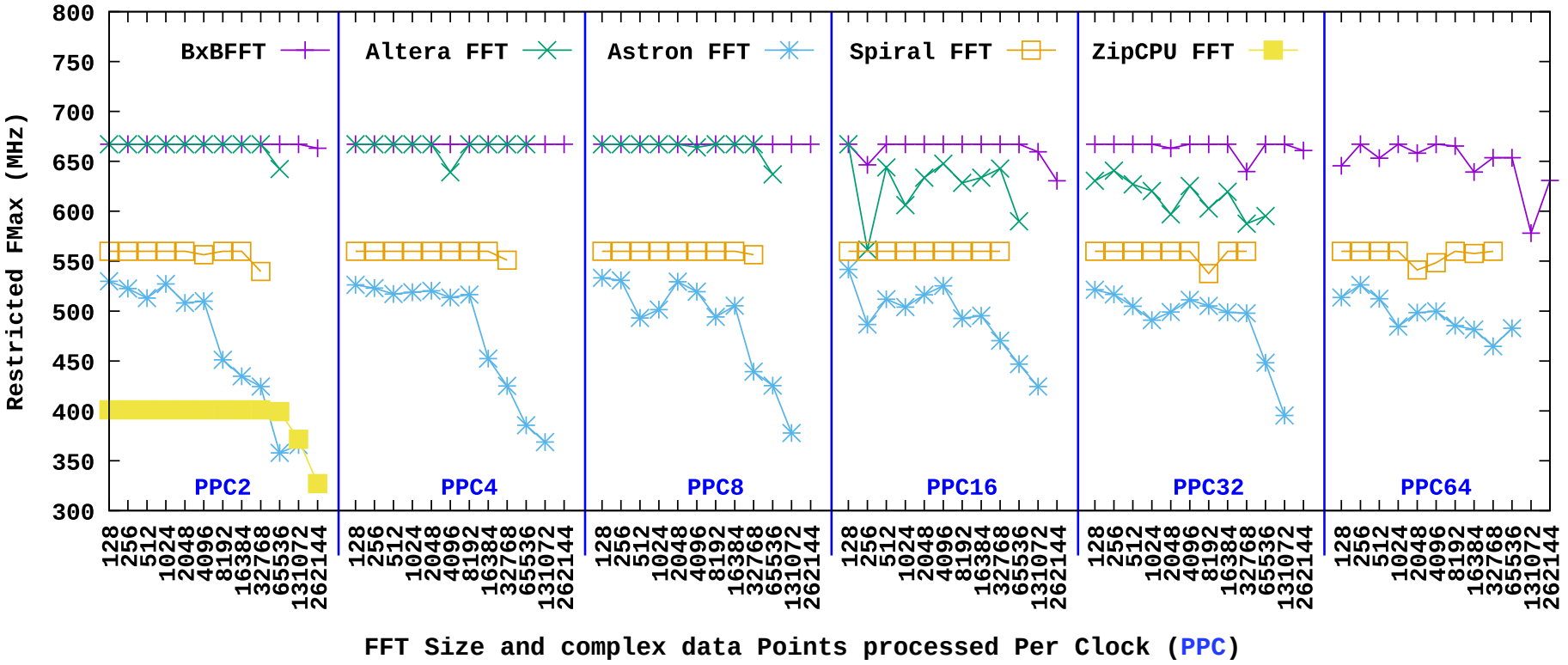
Speed: F_{max} in Xilinx Ultrascale+



BxBFFTs are faster, for large-data problems.

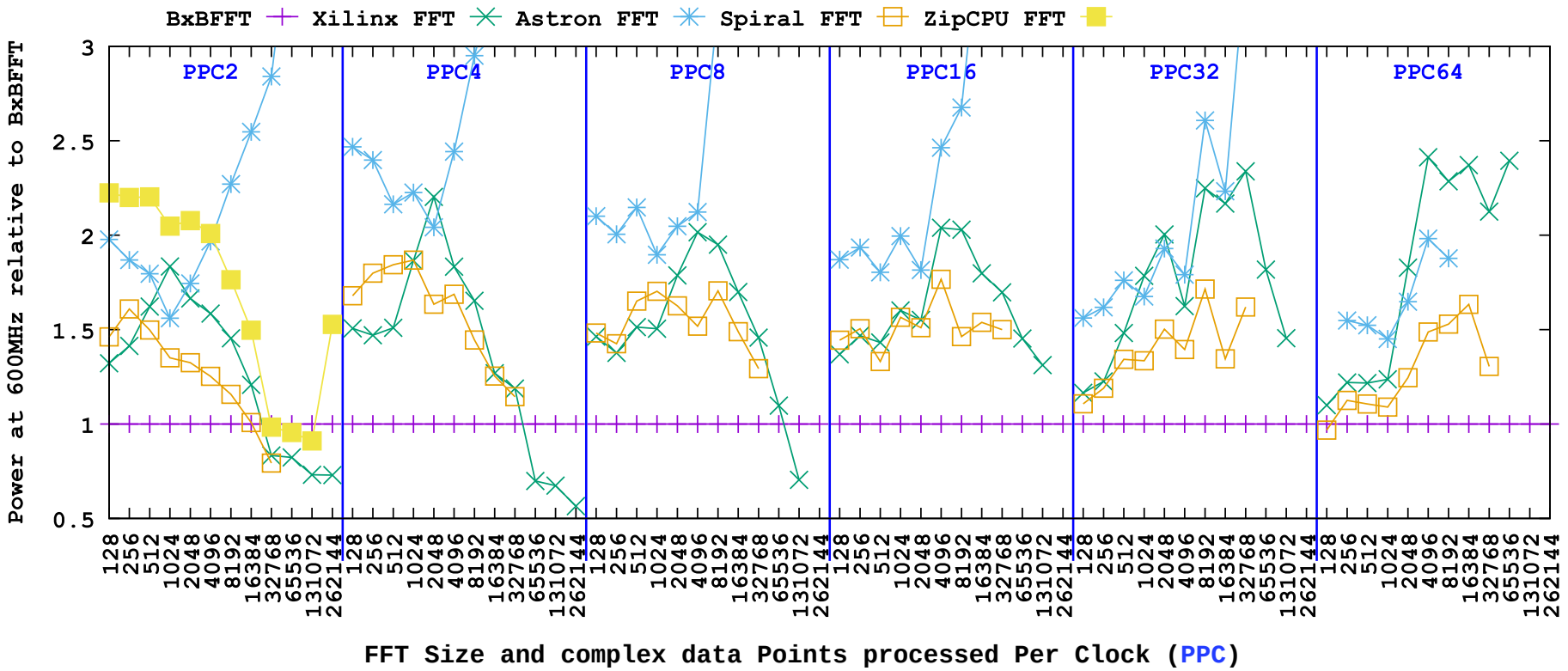
They achieve higher clock rates with more timing margin at greater levels of parallelism.

Speed: F_{max} in Altera Agilex 7



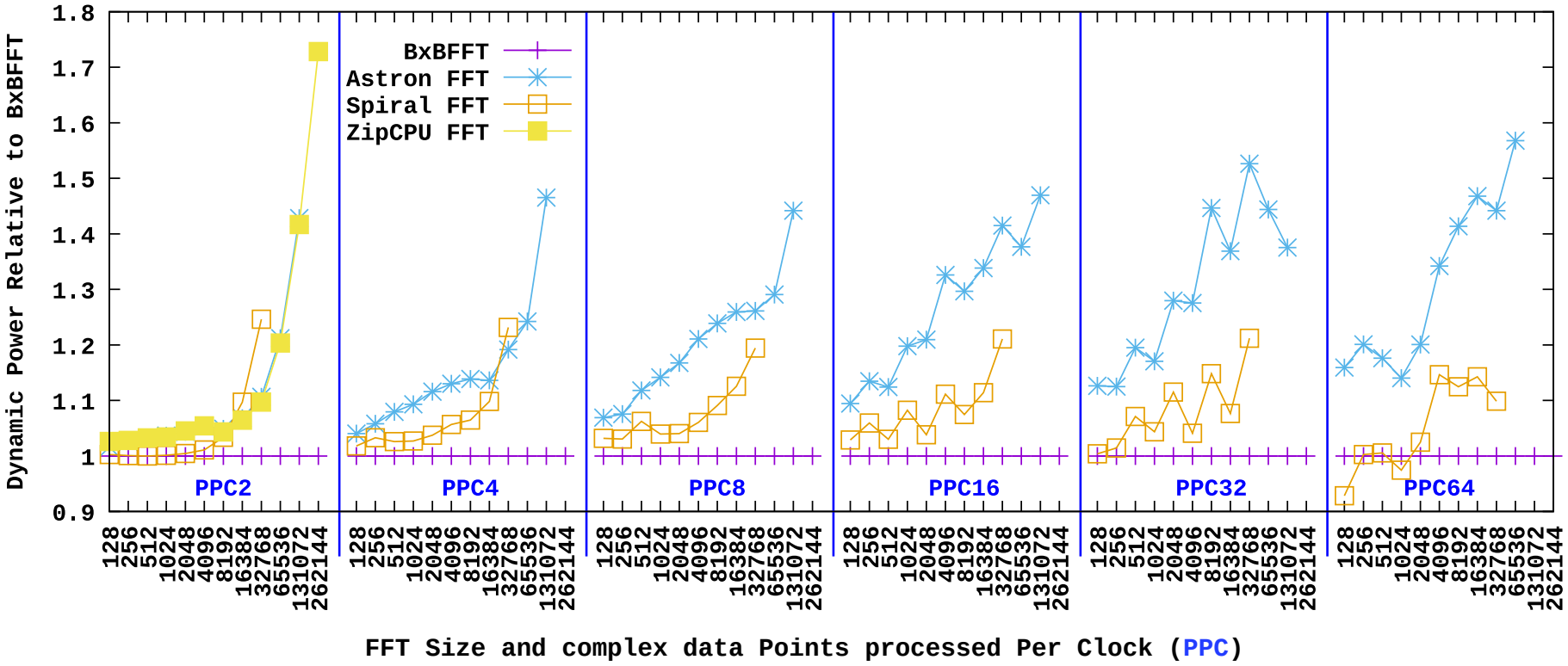
BxBFFTs are faster in Altera FPGAs too.
They'll be faster in an ASIC as well.

Power Efficiency, Xilinx Ultrascale+



BxBFFTs consume 1.5x to 2.0x less power in a Xilinx FPGA.

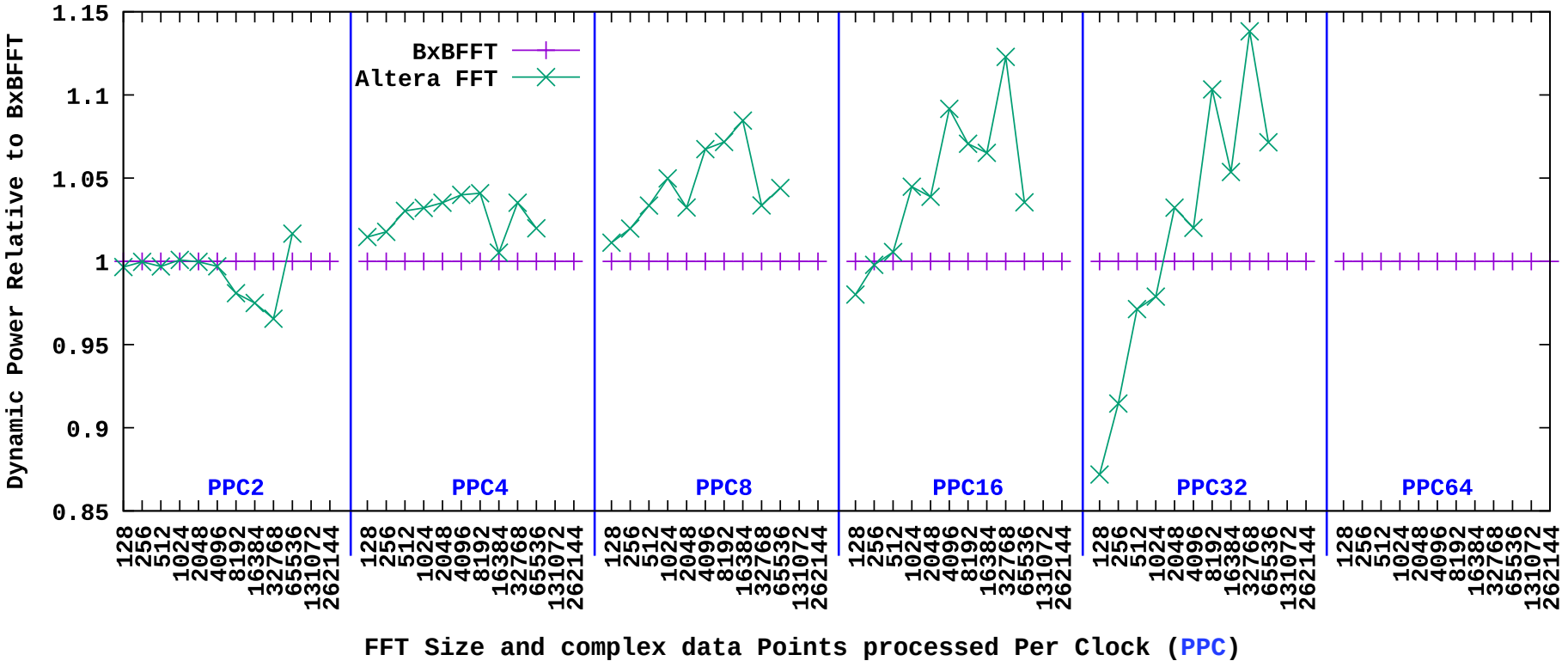
Power Efficiency, Altera Agilex 7



BxBFFTs consume less power in Altera FPGAs than these FFTs, by ~1.1x.

Power Efficiency vs Altera FFT

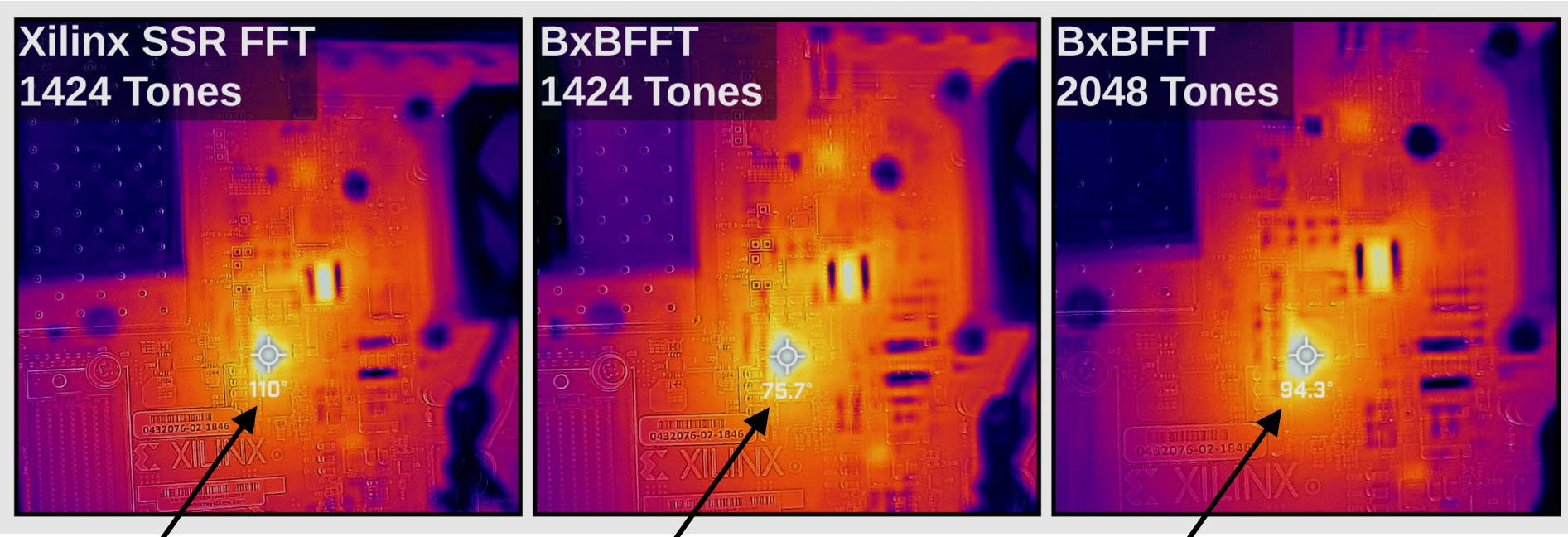
Performance with output data in non-Natural order



The Altera FFT output is bit reversed. An equivalently-configured BxBFFT saves ~1.05x in power.

Power Efficiency Confirmation

FPGA temperature of the same top-level design with different 4096-point PPC=16 FFTs.



110 degrees Celsius

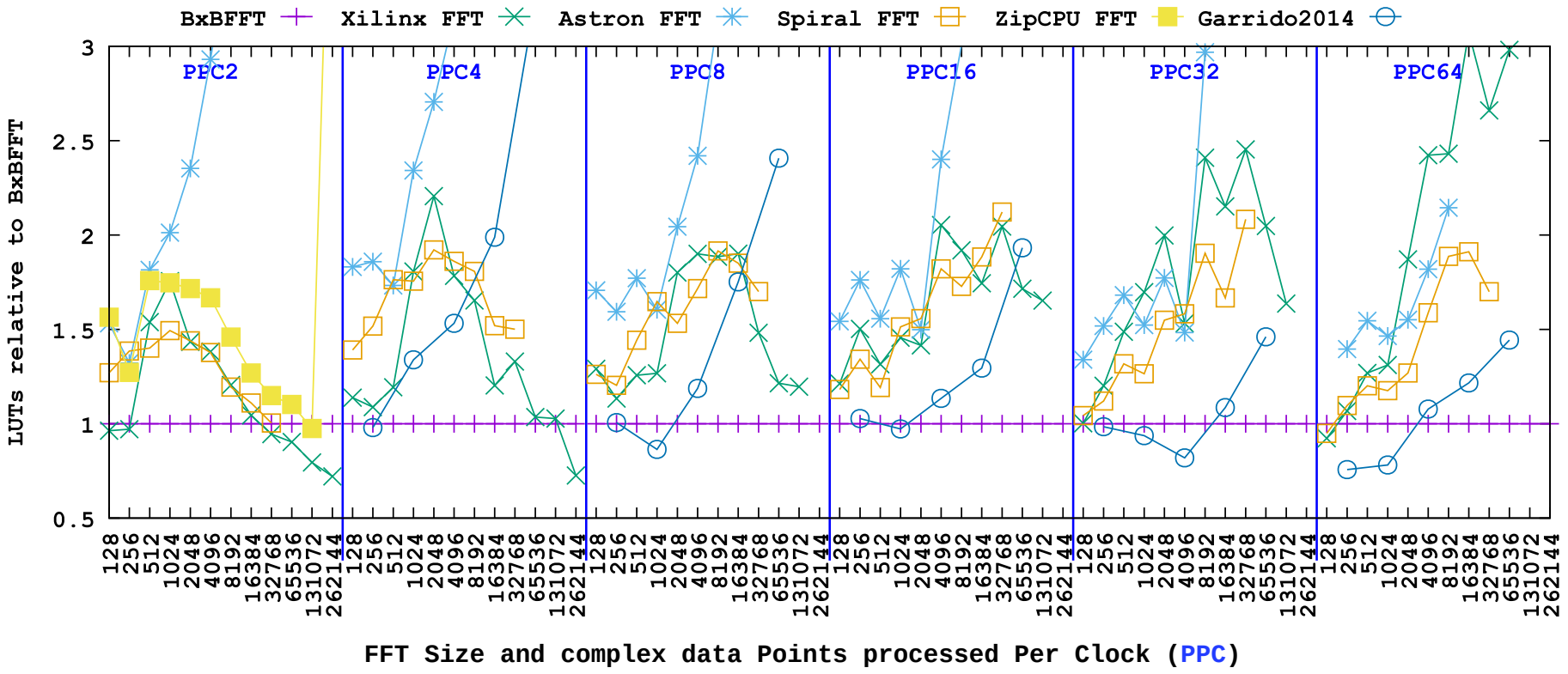
75.7 degrees Celsius

94.3 degrees Celsius

Image Credit: J. Smith, UCSB

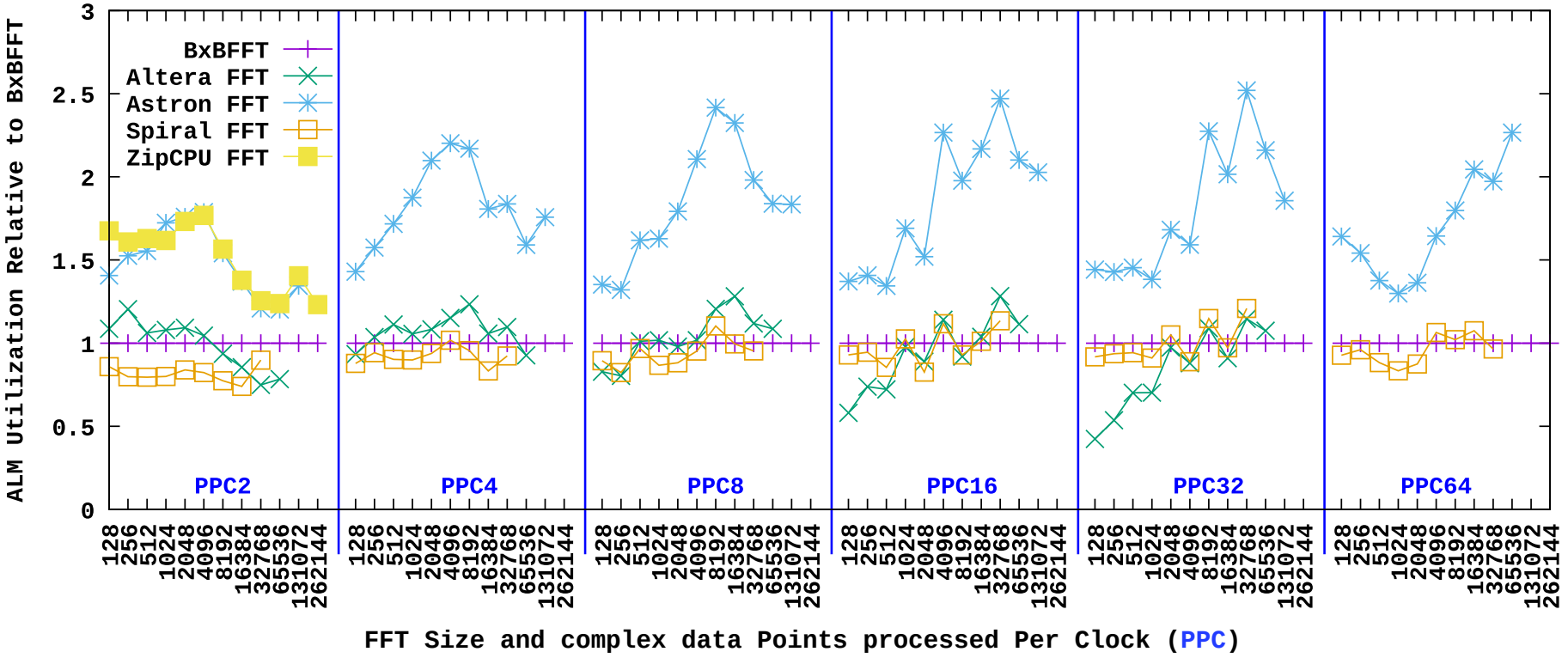
Customer Data showed a 34.3°C thermal drop using a BxBFFT vs a Xilinx SSR FFT. With this savings, the job became possible.

Resource Efficiency: Xilinx LUTs



With a BxBFFT's reduced LUTs, designs fit. Resource contention is also lowered.

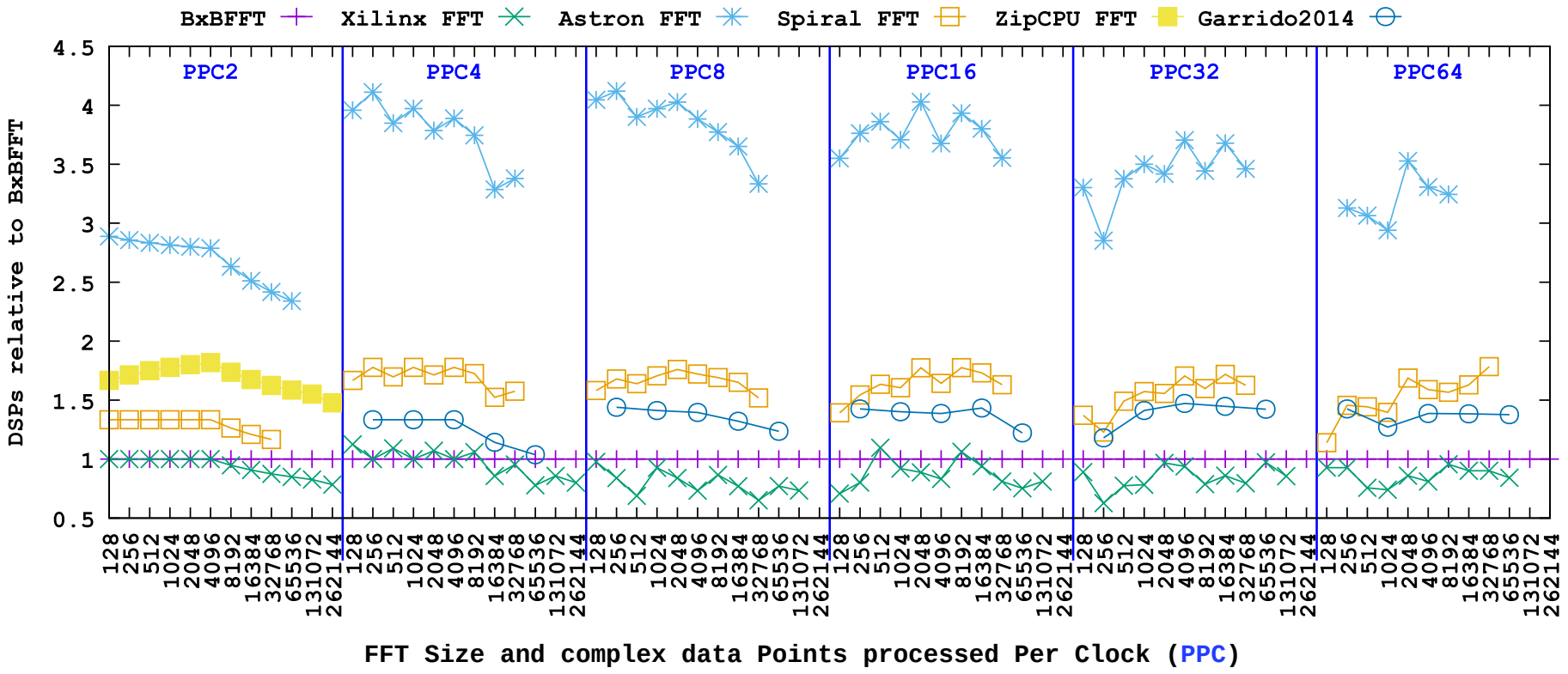
Resource Efficiency: Altera ALMs



Note: Altera FFT has scrambled output data order; an unfair advantage.

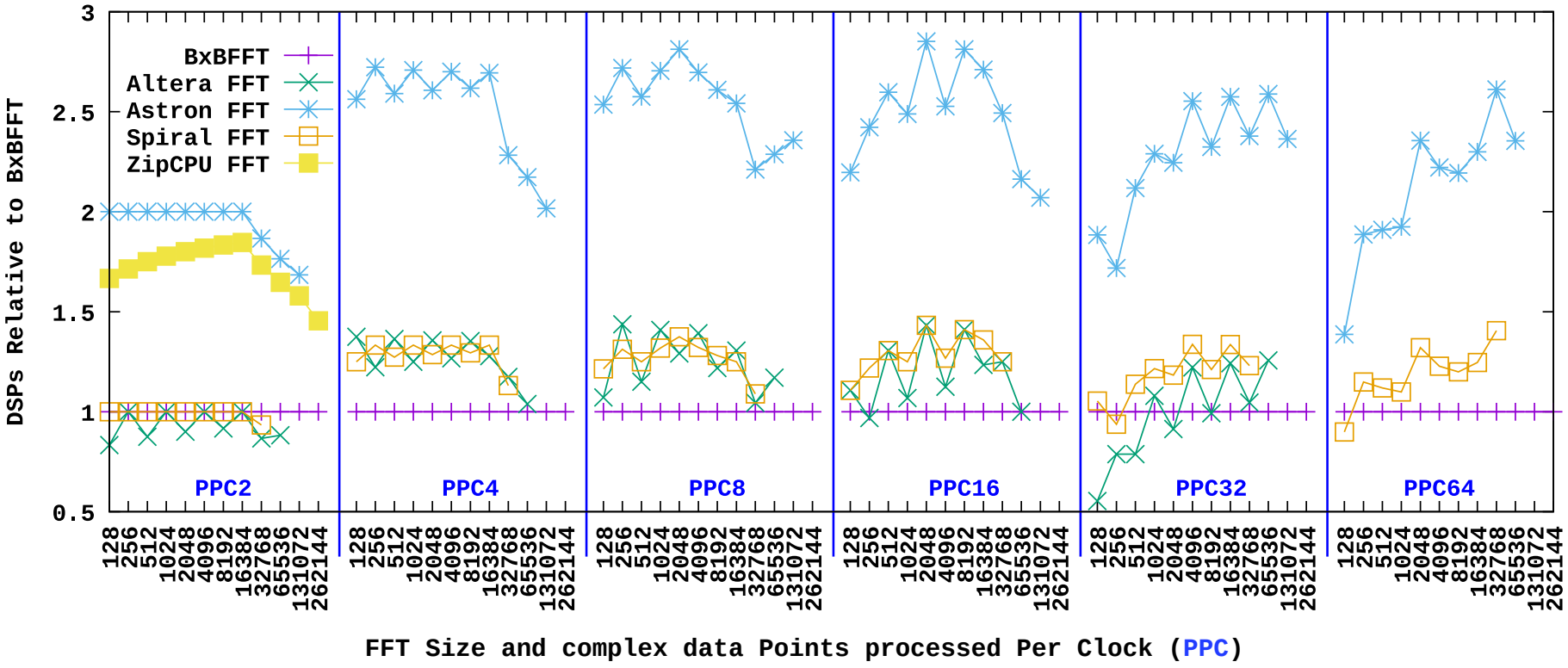
BxBFFT ALMs on Altera are excellent, but other FFTs are also.

Resource Efficiency: Xilinx DSPs



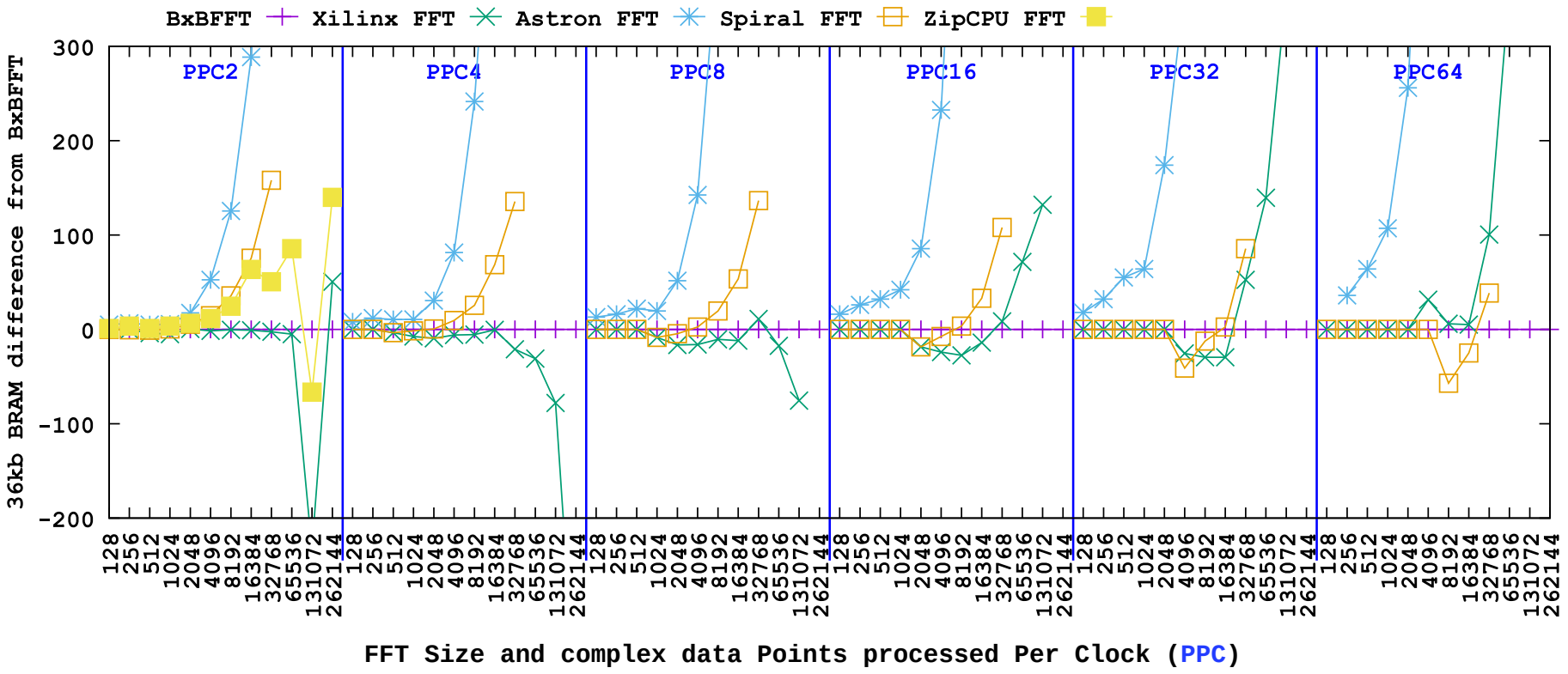
The BxBFFT has excellent DSP performance, although the Xilinx FFT does slightly better.

Resource Efficiency: Altera DSPs



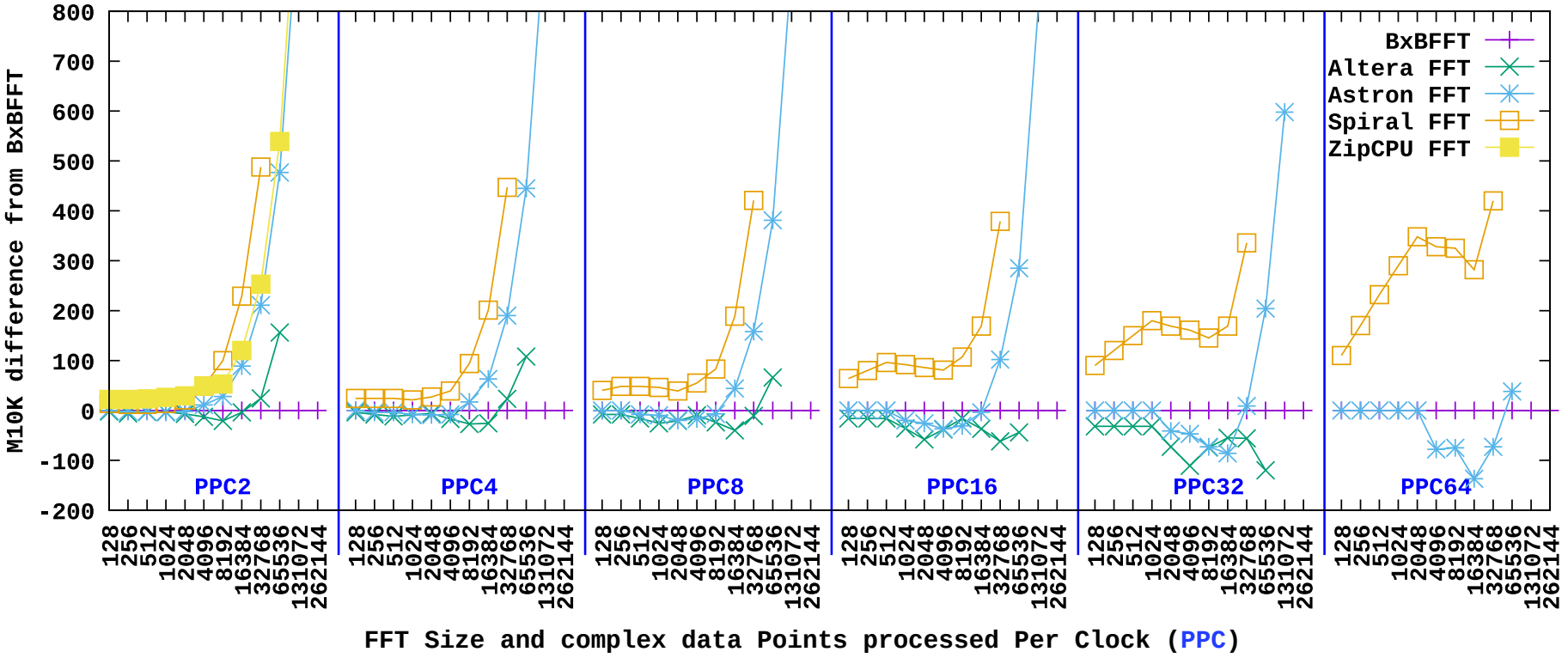
In Altera, the BxBFFT uses ~1.3x fewer DSPs than other FFTs.

Resource Efficiency: Xilinx Memory



BxBFFTs often use less Xilinx memory. A tradeoff of memory size vs speed sometimes gives other FFTs an advantage at a speed cost.

Resource Efficiency: Altera Memory



Note: Altera FFT has scrambled output data order; an unfair advantage.

In both Xilinx and Altera, BxBFFT memory advantages are chiefly at larger FFT sizes.

Feature: Real-to-Complex FFTs

- **Real input data; Complex output data**
- **For spectral processing of raw ADC data**
- **No distortion from real-to-complex filters**
- **Avoid issues with complex sampling**
  - More compact and efficient analog sampling circuits
  - No frequency-dependent I/Q channel balance issues

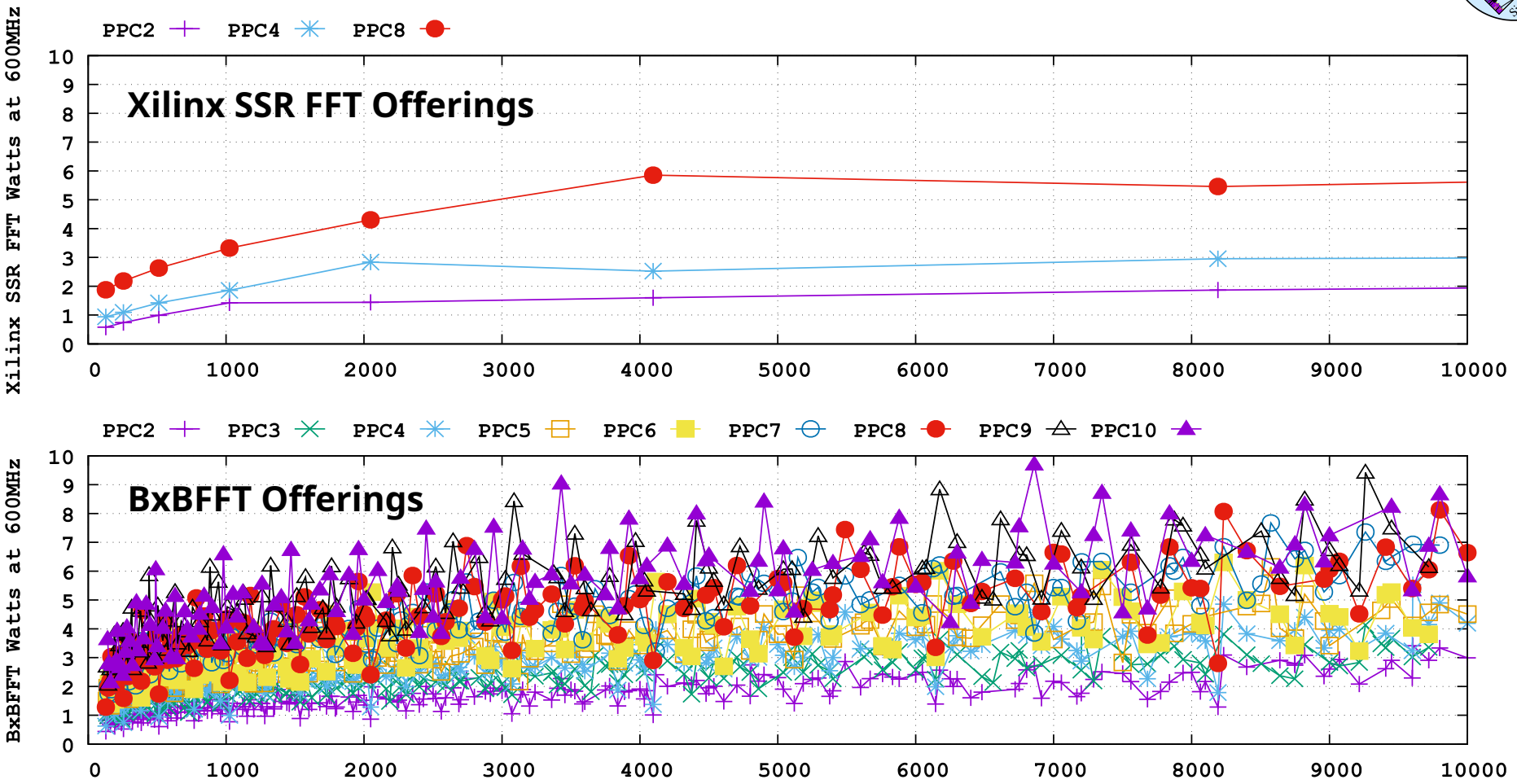
FFTs on real data are enablers of many applications.

Feature: Non-Power-of-2 FFTs

- **Match FFT size to data size**
  - No need to pad data to next power of 2
  - Up to 2x less data in 1D problems, 4x in 2D, 8x in 3D
  - Savings in processing time, memory, power
- **Match FFT parallelism to ADC frequency**
  - Gives less dependence of ADC clock and FPGA clock
  - e.g. Process 60Gsps samples with a 600MHz clock
- **Avoid unusual sampling frequencies**
  - No power-of-2 sampling frequency to get bin spacing
  - Less clock generation circuitry, and simpler circuitry

The BxBFFT makes choosing FFT sizes of 1000, 2000, 3000, etc. easy. These sizes are more natural for many problems.

BxBFFT's Non-Power-of-2 FFTs



BxBFFT Non-Power-of-2 FFT are efficient, with many choices to match your problem.

Feature: Background Reset

- **A full FFT reset**
  - Initializes the BxBFFT at the start of each FFT
- **Does not interrupt processing**
  - No disturbance if the BxBFFT is operating correctly
  - If operation is not correct, full operation is restored
- **Especially useful in difficult environments**
  - e.g. radiation environments, such as space
  - Fixes operation without any need to detect a failure
  - This greatly simplifies error recovery

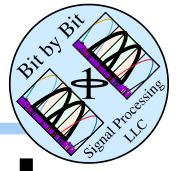
Environments that can induce FPGA errors need reset mechanisms like the BxBFFT's that aid error recovery.

Feature: Data Ordering

- **The BxBFFT supports three data orders:**
  - Scrambled
    - Similar to bit reversed
    - Generalized to support non-power-of-2 radices
    - This data order saves memory and logic
  - Partially Natural
    - From clock-to-clock, samples are sequential
    - Samples each clock are in separate frequency blocks
    - This data order allows cost-free zero padding
  - Fully Natural
    - Samples each clock are sequential
    - From clock-to-clock, sequence continues
    - This data order is simplest and best for most problems

The BxBFFT allows natural orders to simplify processing, or scrambled order to save memory.

Feature: Easy Gain Management



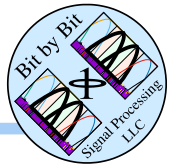
- **Default configuration meets initial needs**
  - Guaranteed overflow prevention
  - Large data bit widths get systems operating quickly
- **Simple gain control optimization**
  - Reduce data bits to save resources and power
  - Specify gain trend to balance SNR and overflow risk
- **Advanced controls are present if needed**
  - Precise control of gain at each stage
  - Optional run-time control of gain
  - Optional overflow measurements at each stage

The BxBFFT has extensive and industry-leading gain controls for easing development, optimizing power, and getting the highest SNR

Features: Miscellaneous (page 1)

- **Convenience**
  - AXI4-S interface and simplified interface support
  - Xilinx Block Design / IP Integrator support
- **Algorithm Development Support**
  - C++ and Matlab models aid algorithm development
- **Quality Assurance**
  - Included delivery tests assure proper operation
  - Included netlist simulations assure proper synthesis
  - Included synthesis results assure performance
- **Verification Support**
  - C++ models support long algorithm verification runs
  - Verilator support speeds up long RTL simulations
- **Third-Party tool support**
  - System Verilog RTL is delivered
  - RTL is generic and tested with multiple tools

Features: Miscellaneous (page 2)

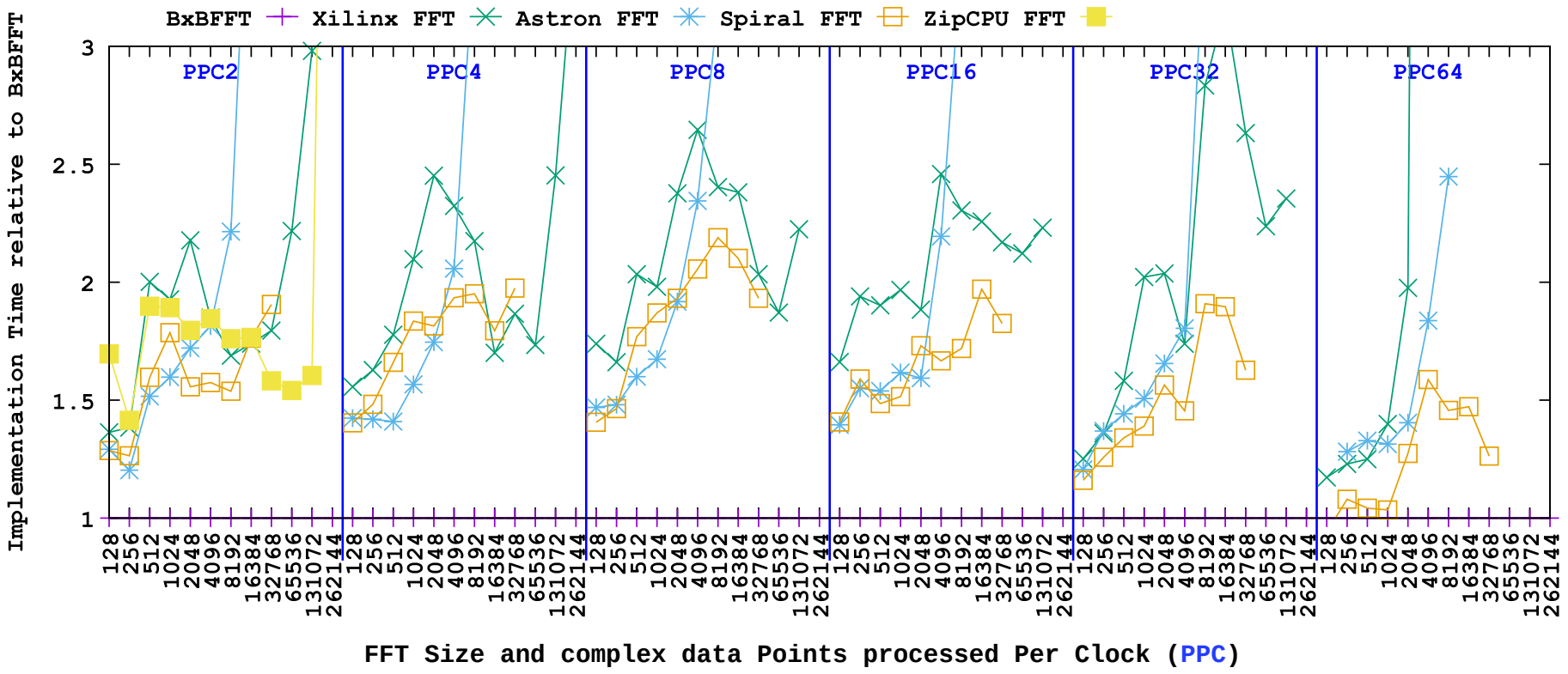


- **Features supporting corner applications**
  - Forward flow control
  - FFT Size variability
  - Multiple FFTs simultaneously
  - Zero time or zero frequency in data center
  - BRAM/URAM tradeoff controls
  - Coefficient tables vs coefficient generation tradeoff
  - Pipelining controls to overcome difficult timing issues
- **BxBFFT works on both Xilinx and Altera**
  - Avoid a single source for FPGA components
- **Extensive documentation**
- **Ongoing development**
- **Support by the original FFT developer**

Time to Market

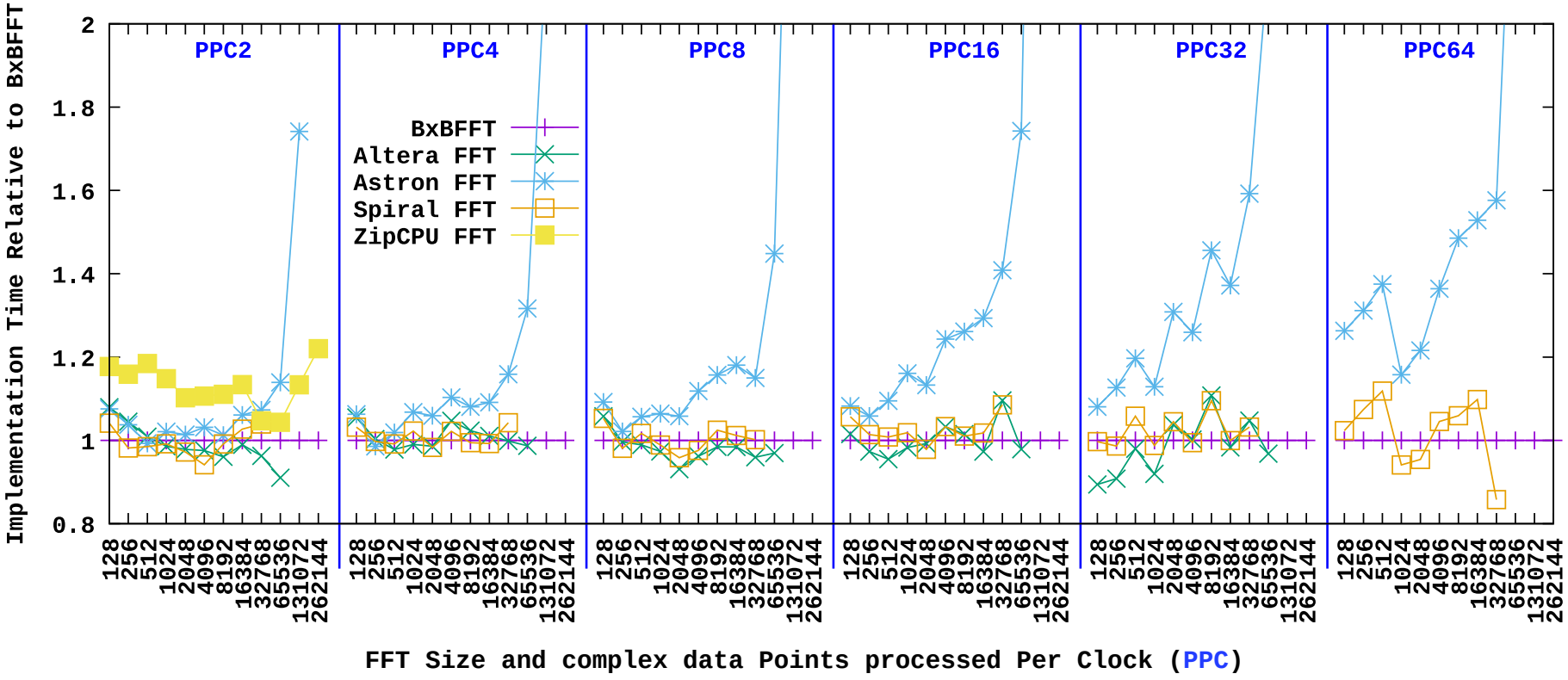
- **BxBFFTs are delivered quickly**
  - Even for unusual sizes
- **BxBFFTs are fast to bring up and integrate**
  - Deliveries include usage examples
  - Provided default settings work for most applications
  - Gain management issues are simplified and clarified
  - BxBFFT RTL synthesizes and simulates faster
- **BxBFFTs ease issues with meeting timing**
  - Industry-leading setup margin
  - Pipelining controls can further increase margin
    - This helps in cases of high resource contention
  - Low BxBFFT resource counts reduce logic contention
- **BxBFFTs have extensive documentation**
- **BxBFFTs have knowledgeable support**

Time to Market: Vivado Run Time



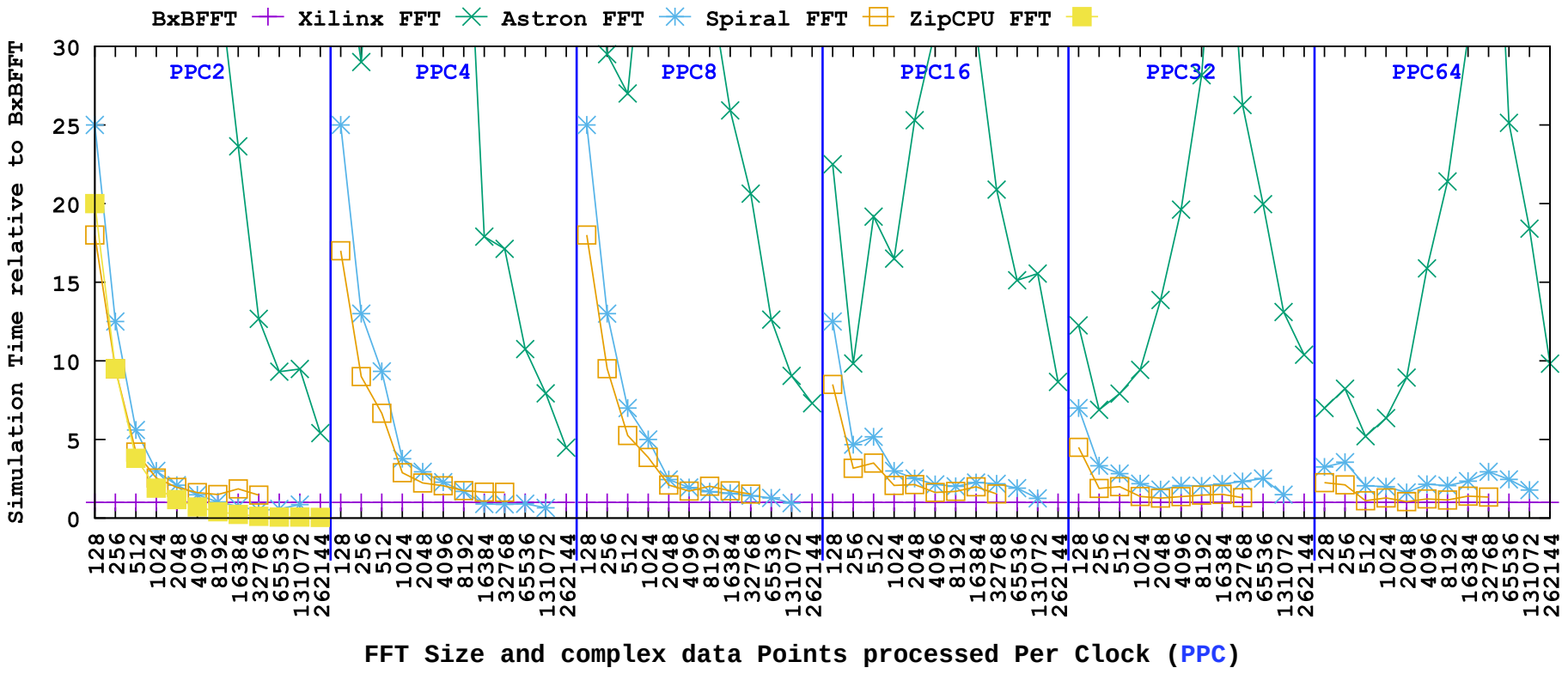
The BxBFFT synthesizes faster in Vivado, saving engineering time.

Time to Market: Quartus Run Time



In Altera FPGAs, BxBFFT synthesis time is also top notch.

Time to Market: Simulation Time



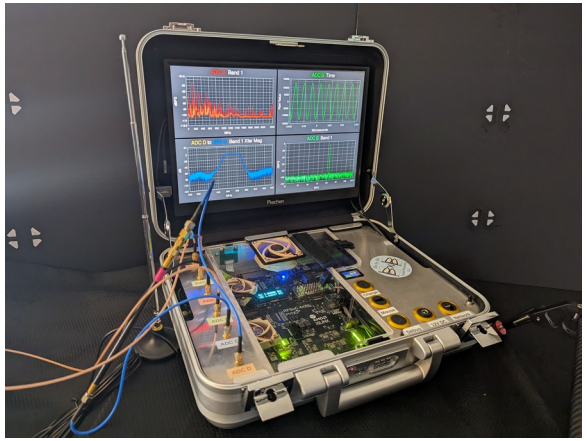
The BxBFFT simulates faster, speeding debugging and verification runs.

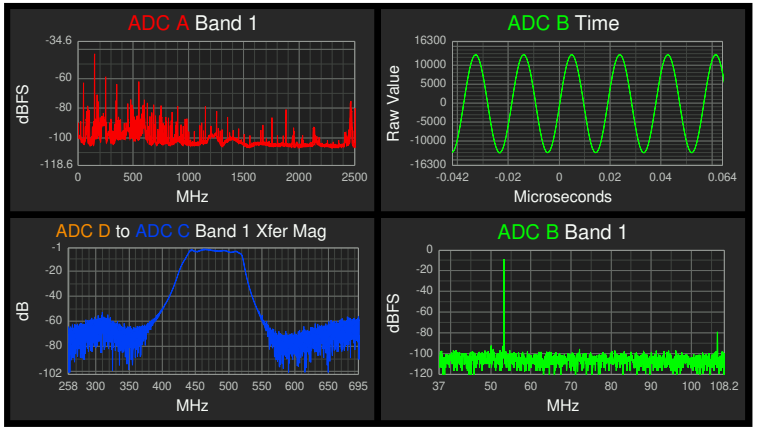
Maturity

- **The BxBFFT is highly mature in Xilinx**
  - Now in its 5th major release
- **Maturity is progressing in Altera**
  - Port complete
  - Tests show excellent performance
    - Better than competitors
    - Not leading by as much as in Xilinx
  - Further optimization may be possible
- **The BxBFFT has a growing customer list**
  - Defense – Spectral Awareness
  - Academia – MKIDs
  - Industry – Lidar

BxBFFT Demonstration

- **Shows a non-power-of-2 real BxBFFT**
  - 96k real points in; 48k complex out
  - 12 Real Points Per Clock in
  - Variable FPGA clock up to 550MHz
  - ADC up to 6.6GHz - beyond 5GHz spec





An example BxBFFT design maximizes timing margin to explore and characterize Xilinx ADCs at sampling rates beyond spec.

BxBFFT Pricing

- **Product Development Pricing**
  - No distribution rights; US$2000 per BxBFFT if 1 or 2, US$1500 for 3 to 8; US$1200 each if more than 9
- **Research/Academic Pricing**
  - No distribution rights; US$1000 per BxBFFT
- **BxBFFTs with Distribution Rights**
  - Unlimited customer products, no end to distribution
  - US$15k each if 1 or 2; US$10k if more than 2
  - US$8k per BxBFFT if more than 9
- **Subscription Plan**
  - Any BxBFFTs you need with distribution rights
  - Prioritized input for new BxBFFT features
  - US$45000 to begin, US$15000/year afterwards
  - Distribution rights end 3 years after subscription end
- **Exceptions possible: Send Justification**

Conclusions

- **The BxBFFT is an awesome FFT**
  - Excellent on all metrics
  - Top on many metrics
- **Top reasons to choose a BxBFFT:**
  - Speed, Efficiency, Feature Support, Time to Market
  - Cross-platform to avoid FPGA single-sourcing
- **BxBFFTs beat free FFTs**
  - Shown on the graphs in this presentation
- **BxBFFTs beat other commercial FFTs**
  - Some of which are shown on the graphs here
  - Competitors don’t post performance comparisons
    - There’s a reason for this!
  - Competitors don’t have the extensive features
    - Sometimes supported features are a patchwork
- **Cheaper and better than in-company FFTs**

About Bit by Bit's Founder

Ross Martin received his PhD in Electrical Engineering from Arizona State University in December, 1994. He worked in Hardware Acceleration for Radar systems, Optical processing, and Communication systems at Lockheed Martin, beginning in 1996 and ending in 2017. His final task was design of a digital switch for communication satellites, based on FFT-based Polyphase Filter Bank (PFB) channelization and beamforming. He started Bit by Bit Signal Processing in 2017 to advance PFB channelization and beamforming technology.